REMARKS/ARGUMENTS

Claims 1 through 10 are pending in the present application. Claims 1, 3 through 6 and 10 have been amended.

The Office Action **(1)** objected to claim 4 for informalities; **(2)** rejected claims 3 and 5 under 35 U.S.C. 112, second paragraph, as being indefinite; **(3)** rejected claims 1 to 4, 7, 8 and 10 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,710,704 to Ando (hereinafter "the Ando reference").

Regarding item **(1)** identified above, it is respectfully submitted that present claim 4 effectively traverses the stated objection and that claim 4 is in condition for allowance.

Regarding item **(2)** identified above, it is respectfully submitted that present claims 3 and 5 effectively traverse the stated rejection. Moreover, it is respectfully submitted that contrary to that which is suggested by the Action, the specification does provide sufficient support for each claim. For instance, the specification provides that the "bit flipping logic circuits 3, 4 and 5 are driven by means of a bit flipping controller 6, which likewise belongs to the means for test pattern generations" (See page 5, lines 1-2), that desired output patterns may be obtained "by means of the bit flipping logic circuit 5 and the bit flipping controller 6" (See page 7, lines 16-18), that "the bit flipping logic circuits 23 to 26 are driven by means of a bit flipping controller 27" (See page 8, lines 1-3), and that "the bit flipping logic circuits and the bit flipping

controller, [may] serve the purpose both of generating test patterns...and of generating desired output patterns" (See page 9, lines 1-4). Thus, based at least on the foregoing, reconsideration and withdrawal of the rejection of claims 3 and 5 are respectfully requested.

Regarding item **(3)** identified above, it is respectfully submitted that claim 1 is patentable over the Ando reference and that the Ando reference, which is directed to IC test equipment, fails to disclose or suggest an arrangement for testing an integrated circuit that has a data word generator for supplying deterministic data words, means for generating a test pattern having one or more bit flipping logic circuits and at least one bit flipping controller for modifying the deterministic data words so that prescribed, deterministic test patterns which can be fed to inputs of the integrated circuit to be tested, are produced, and having comparison means for comparing test output patterns of the integrated circuit with at least one desired output pattern, the arrangement being provided outside the integrated circuit to be tested.

In contrast, the Ando reference teaches that "a test pattern is provided from the test pattern generator 21 to the IC under test 22 (col. 3, lines 29-30)...[t]he test pattern generator 21 [supplying] a control signal generator 29 with a reference clock which is synchronized with the start cycle of a test pattern...the control signal generator 29 derives at its terminal 31 a switch control signal (col. 4, lines 55-60)...[and]...[a] strobe pulse is provided from a terminal 33 (col. 5, lines 16-17). The Ando reference also teaches that "[d]uring the time interval between the moment

immediately after the fall of the strobe pulse and the moment immediately before the generation of the next switch control signal, such a reset signal...is applied from a terminal 35 of the control signal generator 29 to a switch control circuit 36 (col. 5, lines 25-30). Thus, it is respectfully submitted that terminals 31, 33 and 35, which provide a control switch signal, a strobe pulse, and a reset signal, respectively, do not read on "means for test pattern generation having one or more bit flipping logic circuits and at least one bit flipping controller to modify the deterministic data words such that prescribed, deterministic test patterns which can be fed to inputs of the integrated circuit to be tested, are produced". Accordingly, reconsideration and withdrawal of the rejection of claim 1, and allowance thereof, are respectfully requested.

With regard to claims 2 through 5 and claims 7 through 9, which depend either directly or indirectly from claim 1, it is likewise respectfully requested at least for the reasons noted above with respect to claim 1 that the rejections and/or objections relating to claims 2 through 5 be reconsidered and withdrawn, and that such claims be allowed.

With regard to claim 6, it is respectfully submitted that present claim 6 effectively traverses the stated objection. Accordingly, reconsideration and withdrawal of such objection, and allowance of claim 6, are respectfully requested.

With regard to claim 10, it is respectfully submitted that present claim 10 effectively traverses the stated rejection and that the Ando reference at least fails to disclose or suggest a "method

for testing an integrated circuit, in which method deterministic data words are modified via bit flipping logic circuits and at least one bit flipping controller so that prescribed, deterministic test patterns are produced which can be fed to inputs of the integrated circuit to be tested". Accordingly, reconsideration and withdrawal of the rejection of claim 10, and allowance thereof, are respectfully requested.

In sum, it is respectfully submitted that the present claims are patentable over the Ando reference. Hence, this application is in condition for allowance. Accordingly, reconsideration and withdrawal of all rejections, and all objections of the claims, are respectfully requested.

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